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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,226	06/12/2001	Roger May	015114-053300US	7601

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EXAMINER	
SHAH, SAUMIL R	

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,226	MAY ET AL.	
	Examiner	Art Unit	
	Saumil Shah	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because some of the drawings are hand-drawn and not very clear. A proposed drawing correction or corrected drawings are required in reply to the Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Hatanaka et al (US Patent No. 5,418,938) in view of Sugita (US Patent No. 5,276,842).

a. With regard to claim 1, Hatanaka et al disclose a programmable logic integrated circuit comprising:

a programmable logic portion (note figure 3 and column 3, line 36 where an EEPROM is described); and

an embedded processor portion (note column 3, lines 28-29 where the CPUs are described) coupled to the programmable logic portion and comprising:

a processor (note column 3, lines 28-29 where the CPU has a processor); and

a memory block coupled to the processor (note figure 3 where a dual-ported RAM is coupled to the processor) and comprising:

a memory having a first port and a second port (note column 3, line 33 which teaches a dual-ported RAM).

Hatanaka et al fail to disclose a memory block comprising an arbiter coupled to the first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port.

Sugita teaches a memory block comprising an arbiter coupled to the first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port (note column 2, lines 38-40 where the access contention arbitrating circuit teaches an arbiter).

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an arbiter that arbitrates access to the memory as taught by Sugita in the invention of Hatanaka et al since this would have helped avoid access conflicts to an address location and thus preventing wrong data from being stored or retrieved.

4. Claims 2-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatanaka et al (US Patent No. 5,418,938) in view of Sugita (US Patent No. 5,276,842) as applied to claim 1 above, and further in view of Phelan et al (US Patent No. 6,499,089).

a. With regard to claim 2, the combined system of Hatanaka et al/ Sugita disclose each of the features as is described for claim 1 above.

Hatanaka et al/ Sugita fail to disclose the integrated circuit wherein the memory is a dual-port SRAM.

Phelan et al teach an integrated circuit wherein the memory is a dual-port SRAM (note column 1, line 67).

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a dual-port SRAM as taught by Phelan et al in the combined invention of Hatanaka et al/ Sugita since the advantages of SRAM over other RAMs are well known in the art such as faster access and no refresh cycle.

b. With regard to claim 3, the combined system of Hatanaka et al/ Sugita/ Phelan et al disclose each of the features as is described for claim 2 above. Hatanaka et al further teach an integrated circuit wherein the programmable logic portion comprises a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions (note figure 3 and column 3, line 36 where an EEPROM is described. EEPROM is a type of programmable- ROM that consists of a plurality of logical elements that need to be programmed by a programmer according to the function that it needs to perform).

c. With regard to claim 4, the combined system of Hatanaka et al/ Sugita/ Phelan et al disclose each of the features as is described for claim 3 above. Hatanaka et al further teach an integrated circuit wherein the programmable logic portion further comprises a plurality of horizontal and vertical interconnect lines,

programmably coupled to the plurality of logic elements (note figure 3 and column 3, line 36 where an EEPROM is described. EEPROM is a type of programmable- ROM that consists of a horizontal and vertical interconnect lines).

d. With regard to claim 5, the combined system of Hatanaka et al/ Sugita disclose each of the features as is described for claim 1 above.

Hatanaka et al/ Sugita fail to disclose an integrated citcuit wherein the second port is configurable in width and depth.

Phelan et al further teach an integrated circuit wherein the second port is configurable in width and depth (note column 2, lines 11-12 where each one is independently configurable in bit size. Further note, lines 30-32 where each port accesses different blocks and also note column 3, lines 40-48 where the depth of the SRAM block may be changed. These teach that the second port is configurable in width and depth).

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the second port configurable in width and depth as taught by Phelan et al in the invention of Hatanaka et al/ Sugita since this would have allowed the different widths of data to be read out from the memory as per the requirements of the processor. This would not only have made the memory versatile but also have saved costs by implementing a different configuration of memory instead of using a separate memory for the other configuration.

e. With regard to claim 6, the combined system of Hatanaka et al/ Sugita disclose each of the features as is described for claim 1 above.

Hatanaka et al/ Sugita fail to disclose an integrated citcuit wherein the first port and second port are both configurable in width and depth.

Phelan et al further teach an integrated circuit wherein the first port and second port are both configurable in width and depth (note column 2, lines 11-12 where each one is independently configurable in bit size. Further note, lines 30-32 where each port accesses different blocks and also note column 3, lines 40-48 where the depth of the SRAM block may be changed. These teach that both the ports are configurable in width and depth).

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the second port configurable in width and depth as taught by Phelan et al in the invention of Hatanaka et al/ Sugita since this would have allowed the different widths of data to be read out from the memory as per the requirements of the processor. This would not only have made the memory versatile but also have saved costs by implementing a different configuration of memory instead of using a separate memory for the other configuration.

b. With regard to claim 7, Hatanaka et al disclose a programmable logic integrated circuit comprising:

a programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or

registered logic functions (note figure 3 and column 3, line 36 where an EEPROM is described. EEPROM is a type of programmable- ROM that consists of a plurality of logical elements that need to be programmed by a programmer according to the function that it needs to perform); and

an embedded processor portion (note column 3, lines 28-29 where the CPUs are described) coupled to the programmable logic portion and comprising:

a processor (note column 3, lines 28-29 where the CPU has a processor); and

a memory block coupled to the processor (note figure 3 where a dual-ported RAM is coupled to the processor) and comprising:

a first plurality of memory cells for storing data;

a second plurality of memory cells for storing data;

Hatanaka et al fail to disclose a memory block comprising:

a first port couple to the first and second pluralities of memory cells;

a second port coupled to the first and second pluralities of memory cells; and

an arbiter coupled to the first port and the second port, wherein when the second port is accessing the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing

the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells.

Phelan et al teach a memory block comprising:

a first port couple to the first and second pluralities of memory cells;

a second port coupled to the first and second pluralities of memory cells (note column 2, lines 30-35 where the ports access memory blocks independently and may access the same blocks or different blocks).

Phelan et al fail to teach a memory block comprising an arbiter coupled to the first port and the second port, wherein when the second port is accessing the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells.

Sugita teaches a memory block comprising an arbiter coupled to the first port and the second port, wherein when the second port is accessing the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells (note column 2, lines 38-40 where the access contention arbitrating circuit teaches an arbiter. Further note, column 4, lines 8-21 where both the ports try to access the same address and thus the same

plurality of cells. The second port can access any other address apart from the address accessed by the first port).

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a first port and a second port that accesses a first and second plurality of cells as taught by Phelan et al in the invention of Hatanaka et al since this would have allowed each port to access each of the memory cells independently and thus be able to service more requests than a single port SRAM. Furthermore, it would have been obvious to have an arbiter that arbitrates access to the memory as taught by Sugita in the combined invention of Hatanaka et al/ Phelan et al since this would have helped avoid access conflicts to an address location and thus preventing wrong data from being stored or retrieved.

f. With regard to claim 8, the combined invention of Hatanaka et al/ Phelan et al/ Sugita disclose each of the features as is described for claim 7 above. Hatanaka et al further teach the first plurality of memory cells and the second plurality of memory cells are defined by a user-programmable lock register (note column 5, lines 54-67 where the data identification number in the flag area is stored to indicate a lock on the first plurality of cells and can be accessed once the number is cleared).

g. With regard to claims 9-12, the combined system of Hatanaka et al/ Phelan et al/ Sugita teach each of the features as is described in claims 2,3,5,6 and 7 above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Reddy et al (US Patent No. 6,191,998) that teach a programmable logic device memory array circuit having combinable single-port memory arrays.

b. Reams (US Patent No. 6,457,177) that teaches a dual port interactive media system.

c. Plants (US Patent No. 6,496,887) that teaches a SRAM bus architecture and interconnect to an FPGA.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saumil Shah whose telephone number is 703-305-8786. The examiner can normally be reached on 9:00 AM to 5:30 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saurhil Shah
Patent Examiner
AU: 2186

May 6, 2004

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER